NON-VOLATILE MEMORY CELL ARRAY HAVING DISCONTINUOUS SOURCE AND DRAIN DIFFUSIONS CONTACTED BY CONTINUOUS BIT LINE CONDUCTORS AND METHODS OF FORMING

ABSTRACT OF THE DISCLOSURE

Rows of memory cells are electrically isolated from one another by trenches formed in the substrate between the rows that are filled with a dielectric, commonly called "shallow trench isolation" or "STI." Discontinuous source and drain regions of the cells are connected together by column oriented bit lines, preferably made of doped polysilicon, that extend in the column direction on top of the substrate. This structure is implemented in a flash memory array of cells having either one floating gate per cell or at least two floating gates per cell. A process of making a dual-floating gate memory cell array includes etching the word lines twice along their lengths, once to form openings through which source and drain implants are made and in which the conductive bit lines are formed, and second to form individual floating gates with a select transistor gate positioned between them that also serves to erase charge from the adjacent floating gates.